AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph at page 4, lines 7-14, with the following amended paragraph:

Each of the source drivers 30 accepts an input of the image data or incorporates the image data based on the start signal and ~~synchronizing~~ in synchronization with the source driver clock signal, and then [[the]] each source driver 30 converts the image data into corresponding voltage levels to the image data for applying the source signal lines 502 with respective gray-scale voltage signals having the corresponding voltage levels, so that the voltage signals are transmitted through the source signal lines 502 and the thin film transistors to the pixel electrodes.

Please replace the paragraph at page 4, lines 15-20, with the following amended paragraph:

Each of the gate drivers 40 ~~drivers~~ drives the gate signal lines 501 sequentially one-by-one based on the frame start signal and ~~synchronizing~~ in synchronization with the gate driver clock signal. The thin film transistors connected to the gate signal line 501 on the selection are placed ~~in allowing~~ to allow the gray-scale voltage signals to be transmitted from the source signal lines 502 through the thin film transistors to the pixel electrodes.

Please replace the paragraph at page 5, lines 1-6, with the following amended paragraph:

FIG. 2 is a fragmentary block diagram illustrative of a first conventional circuit configuration including a timing controller and source drivers, wherein the circuit configuration is included in the circuit configuration of FIG. 1. FIG. 3 is a view illustrative of contents of image data to be supplied in ~~synchronizing~~ synchronization with a clock signal from the timing controller to the source drivers 30 in FIG. 2.

Please replace the paragraph at page 5, lines 7-16, with the following amended paragraph:

The display control unit 202 includes a timing controller [[202-A]] 202A shown in FIG. 2. The timing controller [[202-A]] 202A has a clock port "[[CLOCK]]clock signal", from which the source driver clock signal is supplied to the source drivers 30. The timing controller [[202-A]] 202A also has a first data port "[[PORT-]]A-port", from which odd-number image data for the pixels of odd numbers [[are]] is supplied to the source drivers 30. The timing controller [[202-A]] 202A also has a second data port "[[PORT-]]B-port", from which even-number image data for the pixels of even numbers [[are]] is supplied to the source drivers 30. The odd-number image data may be referred to as "A-port image data" and the even-number image data may be referred to as "B-port image data".

Please replace the paragraph at page 5, line 17 - page 6, line 2, with the following amended paragraph:

As shown in FIG. 3, the image data includes [[read]]red-color data of 8-bits, green-color data of 8-bits, and blue-color data of 8-bits. For the 8-bits data, eight signal lines are provided. The image data [[are]] is isolated into the odd-number image data and the even-number image data. Namely, each of the [[read]]red-color, green-color, and blue-color data is isolated into the odd-number image data [[and]] or the even-number image data. The odd-number image data (or [[the]] A-port image data) comprises plural sets of the [[read]]red-color, green-color, and blue-color data for the odd-number pixels. The even-number image data (or [[the]] B-port image data) comprises plural sets of the [[read]]red-color, green-color, and blue-color data for the even-number pixels.

Please replace the paragraph at page 6, lines 3-11, with the following amended paragraph:

The timing controller [[202-A]] 202A generates a clock signal "[[CLOCK]]clock signal" having the same cyclic frequency as a data rate of the above image data. The image data and the clock signal are supplied from the timing controller 202-A to the source drivers 30, so that each of the source drivers 30 incorporates the image data at a timing of a rising edge timing of the clock signal for generating corresponding gray-scale voltages to the image data, whereby each of the source drivers 30 applies the gray-scale voltages onto the source signal lines 502. The above

A-port data, the B-port data, and the clock signal are common signals to all of the source drivers 30.

Please replace the paragraph at page 6, lines 12-17, with the following amended paragraph:

FIG. 4 is a fragmentary block diagram illustrative of a second conventional circuit configuration including a timing controller and source drivers, wherein the circuit configuration is included in the circuit configuration of FIG. 1. FIG. 5 is a view illustrative of contents of image data to be supplied in ~~synchronizing~~ synchronization with a clock signal from the timing controller to the source drivers in FIG. 4.

Please replace the paragraph at page 6, line 18 - page 7, line 5, with the following amended paragraph:

The display control unit 202 includes a timing controller [[202-B]] 202B shown in FIG. 4. The timing controller [[202-B]] 202B has a clock port "[[CLOCK]]clock signal", from which the source driver clock signal is supplied to all of the source drivers 3B1, 3B2, 3B3, 3B4, ----. The timing controller [[202-B]] 202B also has a first data port "[[PORT-]]A-port", from which A-port image data [[are]] is supplied to the source drivers 3B1, 3B3, ----. The timing controller [[202-B]] 202B also has a second data port "[[PORT-]]B-port", from which B-port image data [[are]] is supplied to the source drivers 3B1, 3B3, ----. The timing controller [[202-

B]] 202B also has a third data port "[[PORT-]]C-port", from which C-port image data [[are]] is supplied to the source drivers 3B2, 3B4, ----. The timing controller [[202-B]] 202B also has a fourth data port "[[PORT-]]D-port", from which D-port image data [[are]] is supplied to the source drivers 3B2, 3B4, ----.

Please replace the paragraph at page 7, line 18 - page 8, line 1, with the following amended paragraph:

The timing controller [[202-B]] 202B generates a clock signal "[[CLOCK]]clock signal" having the same cyclic frequency as a data rate of the above image data. The timing controller [[202-B]] 202B also generates the A-port data, the B-port data, the C-port data, and the D-port data, wherein the image data comprises plural sets of four-data units. First ~~two-data-units~~ two-data units are divided into the even numbers and the odd numbers as the A-port data and the B-port data. Second ~~two-data-units~~ two-data units are divided into the even numbers and the odd numbers as the C-port data and the D-port data.

Please replace the paragraph at page 8, lines 2-9, with the following amended paragraph:

The image data and the clock signal are supplied from the timing controller [[202-B]] 202B to the source drivers 3B1, 3B2, 3B3, 3B4, ----, so that each of the source drivers 3B1, 3B2, 3B3, 3B4, ---- incorporates the image data at a timing of a rising edge timing of the clock signal

for generating corresponding gray-scale voltages to the image data, whereby each of the source drivers 3B1, 3B2, 3B3, 3B4, ---- applies the gray-scale voltages onto the source signal lines 502. The clock signal [[are]] is a common signal[[s]] to all of the source drivers 3B1, 3B2, 3B3, 3B4, ----.

Please replace the paragraph at page 8, lines 10-15, with the following amended paragraph:

FIG. 6 is a fragmentary block diagram illustrative of a third conventional circuit configuration including a timing controller and source drivers, wherein the circuit configuration is included in the circuit configuration of FIG. 1. FIG. 7 is a view illustrative of contents of image data to be supplied in ~~synchronizing~~ synchronization with a clock signal from the timing controller to the source drivers in FIG. 6.

Please replace the paragraph at page 8, lines 16-24, with the following amended paragraph:

The display control unit 202 includes a timing controller [[202-C]] 202C shown in FIG. 6. The timing controller [[202-C]] 202C has a first clock port "~~CLOCK-1~~clock signal 1", from which a first source driver clock signal is supplied to odd-number source drivers 3B1, 3B3, ----. The timing controller [[202-C]] 202C has a second clock port "~~CLOCK-2~~clock signal 2", from which a second source driver clock signal is supplied to even-number source drivers 3B2,

3B4, ----. The second source driver clock signal is delayed by a half cycle from the first source driver clock signal, so that the second source driver clock signal is opposite in phase to the first source driver clock signal.

Please replace the paragraph at page 9, lines 1-8, with the following amended paragraph:

The timing controller [[202-C]] 202C also has a first data port "[[PORT-]]A-port", from which A-port image data [[are]] is supplied to the source drivers 3B1, 3B3, ----. The timing controller [[202-C]] 202C also has a second data port "[[PORT-]]B-port", from which B-port image data [[are]] is supplied to the source drivers 3B1, 3B3, ----. The timing controller [[202-C]] 202C also has a third data port "[[PORT-]]C-port", from which C-port image data [[are]] is supplied to the source drivers 3B2, 3B4, ----. The timing controller [[202-C]] 202C also has a fourth data port "[[PORT-]]D-port", from which D-port image data [[are]] is supplied to the source drivers 3B2, 3B4, ----.

Please replace the paragraph at page 9, line 23 - page 10, line 11, with the following amended paragraph:

The timing controller [[202-C]] 202C generates the first and second clock signals "~~CLOCK-1~~clock signal 1" and "~~CLOCK-2~~clock signal 2" having the same cyclic frequency as a data rate of the above image data but different in phase by a half cycle from each other, wherein

the first clock signal "~~CLOCK-1~~clock signal 1" is supplied to the odd number source drivers 3B1, 3B3, ----, whilst the second clock signal "~~CLOCK-2~~clock signal 2" is supplied to the even number source drivers 3B2, 3B4, ----. The timing controller [[202-C]] 202C also generates the A-port data, the B-port data, the C-port data, and the D-port data, wherein the image data comprises plural sets of four-data units. First ~~two-data-units~~ two-data units are divided into the even numbers and the odd numbers as the A-port data and the B-port data. Second ~~two-data-units~~ two-data units are divided into the even numbers and the odd numbers as the C-port data and the D-port data, which are delayed by a half cycle from the A-port data and the B-port data.

Please replace the paragraph at page 10, lines 12-23, with the following amended paragraph:

The image data and the clock signal are supplied from the timing controller [[202-C]] 202C to the source drivers 3B1, 3B2, 3B3, 3B4, ----. Each of the odd-number source drivers 3B1, 3B3, ---- incorporates the image data at a timing of a rising edge timing of the first clock signal "~~CLOCK-1~~clock signal 1" for generating corresponding gray-scale voltages to the image data, whereby each of the odd-number source drivers 3B1, 3B3, ---- applies the gray-scale voltages onto the source signal lines 502. Each of the even-number source drivers 3B2, 3B4, ---- incorporates the image data at a half-cycle-delayed timing of the rising edge timing of the second clock signal "~~CLOCK-2~~clock signal 2" for generating corresponding gray-scale voltages to the image data, whereby each of the even-number source drivers 3B2, 3B4, ---- applies the gray-scale voltages onto the source signal lines 502.

Please replace the paragraph at page 10, line 24 - page 11, line 8, with the following amended paragraph:

FIG. 8 is a fragmentary block diagram illustrative of a fourth conventional circuit configuration including a timing controller and source drivers, wherein the circuit configuration is included in the circuit configuration of FIG. 1. FIG. 9 is a view illustrative of contents of image data to be supplied in ~~synchronizing~~ synchronization with a clock signal from the timing controller to the source drivers in FIG. 8. This fourth conventional circuit configuration is disclosed in Japanese laid-open patent publication No. 10-340070. A frequency of the clock signal can be reduced without increasing the width of the data bus for transmitting the image data.

Please replace the paragraph at page 11, lines 9-17, with the following amended paragraph:

The display control unit 202 includes a timing controller [[202-D]] 202D shown in FIG. 8. The timing controller [[202-D]] 202D has a first clock port "~~CLOCK-1~~clock signal 1", from which a first source driver clock signal is supplied to odd-number source drivers 3B1, 3B3, ----. The timing controller [[202-D]] 202D has a second clock port "~~CLOCK-2~~clock signal 2", from which a second source driver clock signal is supplied to even-number source drivers 3B2, 3B4, ----. The second source driver clock signal is delayed by a half cycle from the first source driver clock signal, so that the second source driver clock signal is opposite in phase to the first source driver clock signal.

Please replace the paragraph at page 11, lines 18-22, with the following amended paragraph:

The timing controller [[202-D]] 202D also has a first data port "[[PORT-]]A-port", from which A-port image data [[are]] is supplied to all of the source drivers 3B1, 3B2, 3B3, 3B4, ----. The timing controller [[202-D]] 202D also has a second data port "[[PORT-]]B-port", from which B-port image data [[are]] is supplied to all of the source drivers 3B1, 3B2, 3B3, 3B4, ----.

Please replace the paragraph at page 11, line 23 - page 12, line 9, with the following amended paragraph:

As described above, the image data [[are]] is isolated into two-data systems, for example, odd number data and even number data. The timing controller [[202-D]] 202D generates the first and second clock signals "~~CLOCK-1~~clock signal 1" and "~~CLOCK-2~~clock signal 2" having the same cyclic frequency as a data rate of the above image data but different in phase by a half cycle from each other, wherein the first clock signal "~~CLOCK-1~~clock signal 1" is supplied to the odd-number source drivers 3B1, 3B3, ----, whilst the second clock signal "~~CLOCK-2~~clock signal 2" is supplied to the even-number source drivers 3B2, 3B4, ----. The first and second clock signals "~~CLOCK-1~~clock signal 1" and "~~CLOCK-2~~clock signal 2" have a cyclic frequency corresponding to a half of the data rate of the image data. The timing controller [[202-D]] 202D also generates the A-port data and the B-port data.

Please replace the paragraph at page 12, lines 10-21, with the following amended paragraph:

The image data and the clock signal are supplied from the timing controller [[202-D]] 202D to the source drivers 3B1, 3B2, 3B3, 3B4, ----. Each of the odd-number source drivers 3B1, 3B3, ---- incorporates the image data at a timing of a rising edge timing of the first clock signal "~~CLOCK-1~~clock signal 1" for generating corresponding gray-scale voltages to the image data, whereby each of the odd-number source drivers 3B1, 3B3, ---- applies the gray-scale voltages onto the source signal lines 502. Each of the even-number source drivers 3B2, 3B4, ---- incorporates the image data at a half-cycle-delayed timing of the rising edge timing of the second clock signal "~~CLOCK-2~~clock signal 2" for generating corresponding gray-scale voltages to the image data, whereby each of the even-number source drivers 3B2, 3B4, ---- applies the gray-scale voltages onto the source signal lines 502.

Please replace the paragraph at page 17, lines 7-16, with the following amended paragraph:

The present invention provides a method of driving a liquid crystal display device having a plurality of bus lines for transmitting image data. The method comprises: branching original image data having an original data rate into branched plural-systems image data comprising plural systems having a converted data rate which is equal to either the original data rate or a half of the original data rate; supplying a source driver circuit with the branched plural-systems image data in ~~synchronizing~~ synchronization with at least [[a]] one clock signal having a clock

frequency which is a quarter of the original data rate; and allowing the source driver to further branch the branched plural-systems image data into gray-scale voltage signals.

Please replace the paragraph at page 17, line 17 - page 18, line 3, with the following amended paragraph:

The present invention also provides a circuitry for driving a liquid crystal display device. The circuit comprises: a timing controller for generating image data and at least [[a]] one clock signal; a plurality of data bus lines for transmitting the image data and at least [[a]] one clock signal; and a plurality of source driver circuits for incorporating the image data in ~~synchronizing~~ synchronization with the at least [[a]] one clock signal and converting the image data into gray-scale voltage signals, wherein the timing controller includes: a branching unit for branching original image data having an original data rate into branched plural-systems image data comprising plural systems having a converted data rate which is equal to either the original data rate or a half of the original data rate.

Please replace the paragraph at page 18, lines 17-19, with the following amended paragraph:

FIG. 3 is a view illustrative of contents of image data to be supplied in ~~synchronizing~~ synchronization with a clock signal from the timing controller to the source drivers 30 in FIG. 2.

Please replace the paragraph at page 18, line 24 - page 19, line 2, with the following amended paragraph:

FIG. 5 is a view illustrative of contents of image data to be supplied in ~~synchronizing~~ synchronization with a clock signal from the timing controller to the source drivers in FIG. 4.

Please replace the paragraph at page 19, lines 7-9, with the following amended paragraph:

FIG. 7 is a view illustrative of contents of image data to be supplied in ~~synchronizing~~ synchronization with a clock signal from the timing controller to the source drivers in FIG. 6.

Please replace the paragraph at page 19, lines 14-16, with the following amended paragraph:

FIG. 9 is a view illustrative of contents of image data to be supplied in ~~synchronizing~~ synchronization with a clock signal from the timing controller to the source drivers in FIG. 8.

Please replace the paragraph at page 20, lines 13-15, with the following amended paragraph:

FIG. 17 is a timing chart illustrative of contents of image data to be supplied in ~~synchronizing~~ synchronization with first and second clock signals from the timing controller to the source drivers in FIG. 15.

Please replace the section heading at page 23, line 17, with the following amended section heading:

DETAILED DESCRIPTION OF ~~THE PREFERRED~~ EXEMPLARY EMBODIMENTS

Please replace the paragraph at page 23, line 19 - page 24, line 4, with the following amended paragraph:

A first aspect of the present invention is a method of driving a liquid crystal display device having a plurality of bus lines for transmitting image data. The method comprises: branching original image data having an original data rate into branched plural-systems image data comprising plural systems having a converted data rate which is equal to either the original data rate or a half of the original data rate; supplying a source driver circuit with the branched plural-systems image data in ~~synchronizing~~ synchronization with at least [[a]] one clock signal having a clock frequency which is a quarter of the original data rate; and allowing the source driver to further branch the branched plural-systems image data into gray-scale voltage signals.

Please replace the paragraph at page 24, line 24 - page 25, line 10, with the following amended paragraph:

A second aspect of the present invention is a circuitry for driving a liquid crystal display device. The circuit comprises: a timing controller for generating image data and at least [[a]] one clock signal; a plurality of data bus lines for transmitting the image data and at least [[a]] one clock signal; and a plurality of source driver circuits for incorporating the image data in ~~synchronizing~~ synchronization with the at least [[a]] one clock signal and converting the image data into gray-scale voltage signals, wherein the timing controller includes: a branching unit for branching original image data having an original data rate into branched plural-systems image data comprising plural systems having a converted data rate which is equal to either the original data rate or a half of the original data rate.

Please replace the paragraph at page 26, lines 17-23, with the following amended paragraph:

It is also possible that the data polarity inversion determination circuit further includes: a polarity change detecting ~~circuit~~ unit for detecting polarity change in bit unit of the polarity-inverted image data from the branched plural-systems image data; and a majority determination circuit for determining whether or not the majority of bits of the polarity-inverted image data is different in polarity from the branched plural-systems image data.

Please replace the paragraph at page 26, line 24 - page 27, line 19, with the following amended paragraph:

It is also possible that the timing controller further includes: a first latch circuit for latching the branched plural-systems image data in ~~synchronizing~~ synchronization with the at least [[a]] one clock signal and outputting the branched plural-systems image data as first output data; a first data polarity inversion determination circuit for inverting all bits of the branched plural-systems image data in polarity if a first polarity inversion signal has a predetermined level which indicates polarity inversion, and the first data polarity inversion determination circuit also outputting polarity-inverted image data; a second data polarity inversion determination circuit for comparing the polarity-inverted image data and the branched plural-systems image data to verify whether or not a majority of bits of the polarity-inverted image data is different in polarity from the branched plural-systems image data, and the second data polarity inversion determination circuit also outputting a second polarity inversion signal which has a predetermined level which indicates polarity inversion, if the majority of bits of the polarity-inverted image data is different in polarity from the branched plural-systems image data; and a second latch circuit for latching the second polarity inversion signal in ~~synchronizing~~ synchronization with the at least [[a]] one clock signal and supplying the first polarity inversion signal to the first data polarity inversion determination circuit.

Please replace the paragraph at page 27, line 20 - page 28, line 2, with the following amended paragraph:

It is also possible that the timing controller ~~further~~ furthermore includes: a third latch circuit for latching the polarity-inverted image data in ~~synchronizing~~ synchronization with the at least [[a]] one clock signal and supplying the polarity-inverted image data to the source driver; a fourth latch circuit for latching the first polarity inversion signal in ~~synchronizing~~ synchronization with the at least [[a]] one clock signal and supplying the first polarity inversion signal to the source driver.

Please replace the paragraph at page 30, line 9 - page 31, line 4, with the following amended paragraph:

It is also possible that the serial-to-parallel converting unit further includes: a first latch circuit for latching the converted plural-systems image data in ~~synchronizing~~ synchronization with the at least [[a]] one clock signal and outputting the converted plural-systems image data as first output data; a first data polarity inversion determination circuit for inverting all bits of the converted plural-systems image data in polarity if a first polarity inversion signal has a predetermined level which indicates polarity inversion, and the first data polarity inversion determination circuit also outputting polarity-inverted image data; a second data polarity inversion determination circuit for comparing the polarity-inverted image data and the converted plural-systems image data to verify whether or not a majority of bits of the polarity-inverted image data is different in polarity from the converted plural-systems image data, and the second

data polarity inversion determination circuit also outputting a second polarity inversion signal which has a predetermined level which indicates polarity inversion, if the majority of bits of the polarity-inverted image data is different in polarity from the converted plural-systems image data; and a second latch circuit for latching the second polarity inversion signal in ~~synchronizing~~ synchronization with the at least [[a]] one clock signal and supplying the first polarity inversion signal to the first data polarity inversion determination circuit.

Please replace the paragraph at page 31, lines 5-11, with the following amended paragraph:

It is also possible that the serial-to-parallel converting unit ~~further~~ furthermore includes: a third latch circuit for latching the polarity-inverted image data in ~~synchronizing~~ synchronization with the at least [[a]] one clock signal and supplying the polarity-inverted image data to the source driver; a fourth latch circuit for latching the first polarity inversion signal in ~~synchronizing~~ synchronization with the at least [[a]] one clock signal and supplying the first polarity inversion signal to the source driver.

Please replace the paragraph at page 32, line 14 - page 33, line 4, with the following amended paragraph:

The display panel 5A includes a glass substrate, a plurality of source lines extending in parallel to a row direction, a plurality of gate lines extending in parallel to a column direction, a

matrix array of pixel electrodes at crossing points of the source lines and the gate lines, a matrix array of thin film transistors, a common electrode, and liquid crystal cells between the pixel electrodes and the common electrode. Each of the thin film transistors has a [[drain]] source connected to the source line, a gate electrode connected to the gate line, and a ~~source~~ drain connected to the pixel electrode. The gate line is driven to place the thin film transistor into ON-state, whereby the gray-scale voltage generated by the source driver 3A and transmitted on the source line 52 is supplied through the thin film transistor to the pixel electrode, so that the pixel electrode has the gray-scale voltage. The common electrode is fixed in potential at a predetermined level, for example, a ground level. A potential difference between the pixel electrode and the common electrode depends on the gray-scale voltage.

Please replace the paragraph at page 36, lines 5-14, with the following amended paragraph:

The functions of the timing controller 22A and the source driver 3A are as follows. The timing controller 22A may be integrated in a semiconductor integrated circuit (LSI) which receives various display timing signals, for example, a clock signal, a display timing signal, a horizontal ~~synchronizing~~ synchronization signal and a vertical ~~synchronizing~~ synchronization signal, wherein the display timing signals have been supplied from the graphic controller 11A through the transmitter 12A and the receiver circuit 21A to the timing controller 22A. The timing controller 22A drives the plural source drivers 3A and the plural gate drivers 4A based on the display timing signals and display data.

Please replace the paragraph at page 36, line 22 - page 37, line 9, with the following amended paragraph:

The source drivers 3A comprise a row alignment of source drivers 3A1, 3A2, 3A3, ----, 3AN. Upon input of the start signal 7A, the source drivers 3A1, 3A2, 3A3, ----, 3AN are serial operations from the source driver 3A1 to the source driver 3AN. Each of the source drivers 3A1, 3A2, 3A3, ----, 3AN outputs image data concurrently to the source lines which number is equal to pixel number /N, wherein the pixel number is the number of the pixels on each line. Each of the source drivers 3A receives the image data 6A, the start signal 7A, and the clock signal 8A from the timing controller 22A, so that each of the source drivers 3A operates to latch the image data 6A into an internal ~~resister~~ register thereof at the timing of the clock signal 8A and performs a digital-to-analog conversion of the image data prior to supply of the image signal to the source signal lines 52.

Please replace the paragraph at page 38, lines 13-23, with the following amended paragraph:

The timing controller 22A may comprise a serial-to-parallel converter block 221A, a clock signal generator circuit 222A, and a phase adjuster circuit 223A. The serial-to-parallel converter block 221A receives an input of the image data and an input of a dot-clock signal of a data rate of the image data. The phase adjuster circuit 223A receives an input of the dot-clock signal and an input of ~~synchronizing~~ synchronization signals Vsync, Hsync, and DE. The clock signal generator circuit 222A is electrically coupled to the phase adjuster circuit 223A for

receiving an input of a reset signal from the phase adjuster circuit 223A. The serial-to-parallel converter block 221A is also electrically coupled to the phase adjuster circuit 223A for receiving an input of a reset signal from the phase adjuster circuit 223A.

Please replace the paragraph at page 39, line 20 - page 40, line 6, with the following amended paragraph:

FIG. 12 is a block diagram illustrative of an internal configuration of each of the source drivers shown in FIG. 10. FIG. 13 is a timing chart illustrative of waveforms of various signals to describe operations of the each source driver shown in FIG. 12. FIG. 13 illustrates a waveform of A-port image data for three primary colors outputted from the A-port, a waveform of B-port image data for three primary colors outputted from the B-port, and waveforms of first and second clock signals which are opposite to each other in phase of a half cyclic frequency which corresponds to the data rate of the image data. FIG. 13 further illustrates a waveform of a data [[patch]] <u>latch</u> pulse signal, a polarity signal, and a source driver output signal which is to be applied to the source line.

Please replace the paragraph at page 41, lines 7-16, with the following amended paragraph:

With reference to FIG. 12, each of the source drivers 3A comprises a shift ~~resister~~ <u>register</u> 31A, a data register 32A, a data latch 33A, a level shifter 34A, a digital-to-analog

converter 35A, and an output buffer 36A. The shift ~~resister~~ register 31A receives parallel inputs of the start signal, the first and second clock signals, and the data latch pulse signal. The shift ~~resister~~ register 31A has multiple stages. The start signal is sequentially inputted into the multiple stages in the shift ~~resister~~ register 31A, wherein each of the stages outputs a shifted signal upon input of the start signal, whereby the multiple stages sequentially output the shifted signals upon sequential inputs of the start signal.

Please replace the paragraph at page 41, lines 17-22, with the following amended paragraph:

The data register 32A receives parallel inputs of the A-port image data for the three primary colors and further parallel inputs of the B-port image data for the three primary colors. The shifted signals are also supplied from the multiple stages in the shift ~~resister~~ register 31A into the data register 32A sequentially, so that the received A-port and B-port image data are stored sequentially into ~~resisters~~ registers in the data register 32A.

Please replace the paragraph at page 41, line 23 - page 42, line 1, with the following amended paragraph:

The data latch 33A receives the input of the data latch pulse and another input of the polarity signal. The data latch 33A operates to latch the data stored in the data ~~resister~~ register 32A in a single line unit.

Please replace the paragraph at page 43, lines 4-13, with the following amended paragraph:

The clock generator circuit 222A receives the first and second clock signals based on the dot-clock signal. The clock generator circuit 222A outputs the first and second clock signals and the start signal in ~~synchronizing~~ synchronization with the above outputs of the A-port image data and the B-port image data from the A-port and B-port of the serial-to-parallel converter block 221A. The first and second clock signals and the start signal are supplied to the source drivers 3A. The first and second clock signals have a frequency which is equal to a half of the data rate of the A-port image data and the B-port image data. The start signal is positioned at a top position of the image data.

Please replace the paragraph at page 43, line 14 - page 44, line 2, with the following amended paragraph:

The shift register 31A comprises multiple stages of flip-flop circuits, wherein the number of the stages is the number of the source lines connected to each source driver. The shift register 31A sequentially shifts the start signal on the multiple stages in accordance with the first and second clock signals, whereby the multiple stages of the shift register 31A sequentially generate shifted timing signals which are ~~synchronizing~~ in synchronization with the first and second clock signals. The shifted timing signal rises and falls in ~~synchronizing~~ synchronization with rising and falling edges of the clock signal. The timing signals are sequentially outputted from the multiple stages of the shift register 31A. After the start signal reaches the final stage of

the shift register 31A, then the start signal is shifted to the shift register of the next stage driver in ~~synchronizing~~ synchronization with the next clock signal and subsequently the above operations will be further [[be]] repeated.

Please replace the paragraph at page 44, lines 3-11, with the following amended paragraph:

The data register 32A has a plurality of 8-bits registers, wherein the number of the 8-bits registers is equal to ~~division~~ multiplication of the pixel number by 8. The data register 32A receives parallel inputs of the A-port image data for the three primary colors and further parallel inputs of the B-port image data for the three primary colors. The shifted timing signals are also supplied from the multiple stages in the shift ~~resister~~ register 31A into the data register 32A sequentially, so that the received A-port and B-port image data are stored sequentially into corresponding 8-bits ~~resisters~~ registers for every inputs of the timing signals.

Please replace the paragraph at page 44, lines 12-16, with the following amended paragraph:

The data latch 33A receives the input of the data latch pulse and another input of the polarity signal. The data latch pulse is inputted into the data latch 33A after the image [[date]] data for a single line [[are]] is set into the data register of the source driver. The data latch 33A

operates to latch the data stored in the data ~~resister~~ register 32A upon input of the data latch pulse.

Please replace the paragraph at page 45, lines 1-7, with the following amended paragraph:

The output buffer 36A supplies the gray-scale voltage to the source line in ~~synchronizing~~ synchronization with the data latch pulse. At this time, upon receipt of the data latch pulse, the shifter register is ~~re-set~~ reset for the next data register. In order to avoid application of the gray-scale voltage to the pixel electrode at the fixed polarity, based on the polarity signal, the polarity bit of the data to the data latch is changed for every frame[[s]], whereby for every frame[[s]], the polarity of the gray-scale voltage is changed.

Please replace the paragraph at page 45, lines 8-13, with the following amended paragraph:

The operations of the shift register 31A and the data register 32A are continued with the next start signal of the follower source driver. Each of the sequential operations from the data latch 33A in the single line unit to the output buffer 36A are carried out for the all source drivers concurrently. The display operation for the single source line is also carried out for the all source drivers concurrently.

Please replace the paragraph at page 48, line 23 - page 49, line 8, with the following amended paragraph:

A second embodiment according to the present invention will be described in detail with reference to the drawings. FIG. 15 is a fragmentary block diagram illustrative of a novel circuit configuration including a timing controller and source drivers in a second embodiment in accordance with the present invention. FIG. 16 is a block diagram illustrative of the timing controller shown in FIG. 15. FIG. 17 is a timing chart illustrative of contents of image data to be supplied in ~~synchronizing~~ synchronization with first and second clock signals from the timing controller to the source drivers in FIG. 15. FIG. 18 is a diagram illustrative of data structures of A-port data, B-port data, C-port data, and D-port data shown in FIG. 16.

Please replace the paragraph at page 50, line 17 - page 51, line 8, with the following amended paragraph:

As shown in FIG. 16, the timing controller 22B may comprise a serial-to-parallel converter block 221B, a clock signal generator circuit 222B, a phase adjuster/memory controller circuit 224B, a first memory 225B, and a second memory 226B. The serial-to-parallel converter block 221B receives an input of the image data and an input of a dot-clock signal of a data rate of the image data. The phase adjuster/memory controller circuit 224B receives an input of the dot-clock signal and an input of ~~synchronizing~~ synchronization signals Vsync, Hsync, and DE. The clock signal generator circuit 222B is electrically coupled to the phase adjuster/memory controller circuit 224B for receiving an input of a reset signal from the phase adjuster/memory

controller circuit 224B. The serial-to-parallel converter block 221B is also electrically coupled to the phase adjuster/memory controller circuit 224B for receiving an input of a reset signal from the phase adjuster/memory controller circuit 224B. The clock signal generator circuit 222B receives the dot-clock signal and generates the first and second clock signals.

Please replace the paragraph at page 60, lines 3-12, with the following amended paragraph:

The functions of the timing controller 22C and the source driver 3C are as follows. The timing controller 22C may be integrated in a semiconductor integrated circuit (LSI) which receive various display timing signals, for example, a clock signal, a display timing signal, a horizontal ~~synchronizing~~ synchronization signal, and a vertical ~~synchronizing~~ synchronization signal, wherein the display timing signals have been supplied from the graphic controller 11C through the transmitter 12C and the receiver circuit 21C to the timing controller 22C. The timing controller 22C drives the plural source drivers 3C and the plural gate drivers 4C based on the display timing signals and display data.

Please replace the paragraph at page 60, line 20 - page 61, line 7, with the following amended paragraph:

The source drivers 3C comprise a row alignment of source drivers 3C1, 3C2, 3C3, ----, 3CN. Upon input of the start signal 7C, the source drivers 3C1, 3C2, 3C3, ----, 3CN are serial

operations from the source driver 3C1 to the source driver 3CN. Each of the source drivers 3C1, 3C2, 3C3, ----, 3CN outputs image data concurrently to the source lines which number is equal to pixel number /N, wherein the pixel number is the number of the pixels on each line. Each of the source drivers 3C receives the image data 6C, the start signal 7C, and the clock signal 8C from the timing controller 22C, so that each of the source drivers 3C operates to latch the image data 6C into an internal ~~resister~~ register thereof at the timing of the clock signal 8C and performs a digital-to-analog conversion of the image data prior to supply of the image signal to the source signal lines 52.

Please replace the paragraph at page 63, line 23 - page 64, line 10, with the following amended paragraph:

The serial-to-parallel converter block 221C receives an input of the image data and an input of a dot-clock signal of a data rate of the image data. The phase adjuster/memory controller circuit 223C receives an input of the dot-clock signal and an input of ~~synchronizing~~ synchronization signals Vsync, Hsync, and DE. The clock signal generator circuit 222C is electrically coupled to the phase adjuster/memory controller circuit 223C for receiving an input of a reset signal from the phase adjuster/memory controller circuit 223C. The serial-to-parallel converter block 221C is also electrically coupled to the phase adjuster/memory controller circuit 223C for receiving an input of a reset signal from the phase adjuster/memory controller circuit 223C. The clock signal generator circuit 222C receives the dot-clock signal and generates the first and second clock signals.

Please replace the paragraph at page 69, lines 11-20, with the following amended paragraph:

With reference to FIG. 22, each of the source drivers 3C comprises a shift ~~resister~~ register 31C, a data register 32C, a data latch 33C, a level shifter 34C, a digital-to-analog converter 35C, and an output buffer 36C. The shift ~~resister~~ register 31C receives parallel inputs of the start signal, the first or second clock signal, and the data latch pulse signal. The shift ~~resister~~ register 31C has multiple stages. The start signal is sequentially inputted into the multiple stages in the shift ~~resister~~ register 31C, wherein each of the stages outputs a shifted signal upon input of the start signal, whereby the multiple stages sequentially output the shifted signals upon sequential inputs of the start signal.

Please replace the paragraph at page 69, line 21 - page 70, line 3, with the following amended paragraph:

The data register 32C receives parallel inputs of the A-port or C-port image data for the three primary colors and further parallel inputs of the B-port or D-port image data for the three primary colors. The shifted signals are also supplied from the multiple stages in the shift ~~resister~~ register 31C into the data register 32C sequentially, so that the received A-port and B-port image data or the C-port and D-port image data are stored sequentially into ~~resisters~~ registers in the data register 32C.

Please replace the paragraph at page 70, lines 4-6, with the following amended paragraph:

The data latch 33C receives the input of the data latch pulse and another input of the polarity signal. The data latch 33C operates to latch the data stored in the data ~~resister~~ register 32C in a single line unit.

Please replace the paragraph at page 77, line 23 - page 78, line 8, with the following amended paragraph:

The functions of the timing controller 22D and the source driver 3D are as follows. The timing controller 22D may be integrated in a semiconductor integrated circuit (LSI) which receive various display timing signals, for example, a clock signal, a display timing signal, a horizontal ~~synchronizing~~ synchronization signal, and a vertical ~~synchronizing~~ synchronization signal, wherein the display timing signals have been supplied from the graphic controller 11D through the transmitter 12D and the receiver circuit 21D to the timing controller 22D. The timing controller 22D drives the plural source drivers 3D and the plural gate drivers 4D based on the display timing signals and display data.

Please replace the paragraph at page 78, line 16 - page 79, line 3, with the following amended paragraph:

The source drivers 3D comprise a row alignment of source drivers 3D1, 3D2, 3D3, ----, 3DN. Upon input of the start signal 7D, the source drivers 3D1, 3D2, 3D3, ----, 3DN are serial operations from the source driver 3D1 to the source driver 3DN. Each of the source drivers 3D1, 3D2, 3D3, ----, 3DN outputs image data concurrently to the source lines which number is equal to pixel number /N, wherein the pixel number is the number of the pixels on each line. Each of the source drivers 3D receives the image data 6D, the start signal 7D, and the clock signal 8D from the timing controller 22D, so that each of the source drivers 3D operates to latch the image data 6D into an internal ~~resister~~ register thereof at the timing of the clock signal 8D and performs a digital-to-analog conversion of the image data prior to supply of the image signal to the source signal lines 52.

Please replace the paragraph at page 81, line 24 - page 82, line 11, with the following amended paragraph:

The serial-to-parallel converter block 221D receives an input of the image data and an input of a dot-clock signal of a data rate of the image data. The phase adjuster/memory controller circuit 223D receives an input of the dot-clock signal and an input of ~~synchronizing~~ synchronization signals Vsync, Hsync, and DE. The clock signal generator circuit 222D is electrically coupled to the phase adjuster/memory controller circuit 223D for receiving an input of a reset signal from the phase adjuster/memory controller circuit 223D. The serial-to-parallel

converter block 221D is also electrically coupled to the phase adjuster/memory controller circuit 223D for receiving an input of a reset signal from the phase adjuster/memory controller circuit 223D. The clock signal generator circuit 222D receives the dot-clock signal and generates the first and second clock signals.

Please replace the paragraph at page 85, lines 10-20, with the following amended paragraph:

FIG. 28 is a block diagram illustrative of an internal configuration of each of the source drivers shown in FIG. 25. Each of the source drivers 3D comprises a shift ~~resister~~ register 31D, a data register 32D, a data latch 33D, a level shifter 34D, a digital-to-analog converter 35D, and an output buffer 36D. The shift ~~resister~~ register 31D receives parallel inputs of the start signal, the first or second clock signal, and the data latch pulse signal. The shift ~~resister~~ register 31D has multiple stages. The start signal is sequentially inputted into the multiple stages in the shift ~~resister~~ register 31D, wherein each of the stages outputs a shifted signal upon input of the start signal, whereby the multiple stages sequentially output the shifted signals upon sequential inputs of the start signal.

Please replace the paragraph at page 85, line 21 - page 86, line 3, with the following amended paragraph:

The data register 32D receives parallel inputs of the A-port or C-port image data for the three primary colors and further parallel inputs of the B-port or D-port image data for the three primary colors. The shifted signals are also supplied from the multiple stages in the shift ~~resister~~ register 31D into the data register 32D sequentially, so that the received A-port and B-port image data or the C-port and D-port image data are stored sequentially into ~~resisters~~ registers in the data register 32D.

Please replace the paragraph at page 86, lines 4-6, with the following amended paragraph:

The data latch 33D receives the input of the data latch pulse and another input of the polarity signal. The data latch 33D operates to latch the data stored in the data ~~resister~~ register 32D in a single line unit.

Please replace the paragraph at page 94, lines 7-15, with the following amended paragraph:

The first bus data BUS-A1-A24 comprises 24-bits, which further comprises three sets of 8-bits for primary colors[[,]] [[read]]red, green, and blue. The second bus data BUS-B1-B24 also comprises 24-bits, which further comprises three sets of 8-bits for primary colors[[,]]

[[read]]red, green, and blue. The third bus data BUS-C1-C24 also comprises 24-bits, which further comprises three sets of 8-bits for primary colors[[,]] [[read]]red, green, and blue. The fourth bus data BUS-D1-D24 also comprises 24-bits, which further comprises three sets of 8-bits for primary colors[[,]] [[read]]red, green, and blue. A 256-gray-scale[[s]] display is realized.

Please replace the paragraph at page 94, line 16 - page 95, line 5, with the following amended paragraph:

Operation[[s]] of the driver circuit shown in FIG. 31 will be described. The first bus data BUS-A1-A24, the second bus data BUS-B1-B24, the first polarity inversion signal INV-A, and the second polarity inversion signal INV-B are outputted from the timing controller 2E in ~~synchronizing~~ synchronization with the first clock signal CLK1. The first bus data BUS-A1-A24, the second bus data BUS-B1-B24, the first polarity inversion signal INV-A, and the second polarity inversion signal INV-B are supplied to each of the odd-number source drivers 3-1, 3-3, ---- on the odd-number stages. Further, the first control signal SP1 is supplied to each of the odd-number source drivers 3-1, 3-3, ---- on the odd-number stages. At the timing of the input of the first control signal SP1, each of the odd-number source drivers 3-1, 3-3, ---- latches the first bus data BUS-A1-A24, the second bus data BUS-B1-B24, the first polarity inversion signal INV-A, and the second polarity inversion signal INV-B.

Please replace the paragraph at page 95, line 15 - page 96, line 3, with the following amended paragraph:

The third bus data BUS-C1-C24, the fourth bus data BUS-D1-D24, the third polarity inversion signal INV-C_2 and the fourth polarity inversion signal INV-D are outputted from the timing controller 2E in ~~synchronizing~~ synchronization with the second clock signal CLK2. The third bus data BUS-C1-C24, the fourth bus data BUS-D1-D24, the third polarity inversion signal INV-C_2 and the fourth polarity inversion signal INV-D are supplied to each of the even number source drivers 3-2, 3-4, ---- on the even-number stages. Further, the second control signal SP2 is supplied to each of the even-number source drivers 3-2, 3-4, ---- on the even-number stages. At the timing of the input of the second control signal SP2, each of the even-number source drivers 3-2, 3-4, ---- latches the third bus data BUS-C1-C24, the fourth bus data BUS-D1-D24, the third polarity inversion signal INV-C_2 and the fourth polarity inversion signal INV-D.

Please replace the paragraph at page 96, lines 13-22, with the following amended paragraph:

Each of the source drivers [[31-]]3-1, 3-2, 3-3, 3-4, ---- also receives a respective driving start signal which is not illustrated. Upon receipt of the respective driving start signal, each of the odd-number source drivers 3-1, 3-3, ---- generates a gray-scale voltage based on the first bus data BUS-A1-A24 and the second bus data BUS-B1-B24. Upon receipt of the respective driving start signal, each of the even-number source drivers 3-2, 3-4, ---- generates a gray-scale voltage based on the third bus data BUS-C1-C24 and the fourth bus data BUS-D1-D24. The gray-scale

voltages are supplied to the liquid crystal panel 5E, whereby the liquid crystal panel 5E performs the display based on the gray-scale voltages.

Please replace the paragraph at page 100, line 13 - page 101, line 3, with the following amended paragraph:

FIG. 33 is a timing chart illustrative of waveforms of the first and second clock signals CLK1 and CLK2, the bus data BUS1-48, the bus data BUS49-96, the first bus data BUS-A1-A24, the second bus data BUS-B1-B24, the third bus data BUS-C1-C24, and the fourth bus data BUS-D1-D24. The bus data BUS1-48 changes in ~~synchronizing~~ synchronization with the rising edges of the first clock signal CLK1 or at timings PA1, PA2, PA3, ----. The ~~change in synchronizing with the falling edges of th~~ first bus data BUS-A1-A24 and the second bus data BUS-B1-B24 change in synchronization with the falling edges of the first clock signal CLK1 or at timings PB1, PB2, PB3, ----. The bus data BUS49-96[[8]] changes in ~~synchronizing~~ synchronization with the rising edges of the second clock signal CLK2 or at timings PB1, PB2, PB3, ----. The third bus data BUS-C1-C24 and the fourth bus data BUS-D1-D24 change in ~~synchronizing~~ synchronization with the falling edges of the second clock signal CLK2 or at timings PA1, PA2, PA3, ----. The first and second clock signals CLK1 and CLK2 are different in phase from each other by 180 degrees or a half cycle.

Please replace the paragraph at page 102, line 23 - page 103, line 8, with the following amended paragraph:

The clock signal "clk" is inputted into the clock input terminal of each of the D-flip-flop circuits 13-1, 13-2, ---, 13-24, the D-flip-flop circuits 14-1, 14-2, ---, 14-24, the D-flip-flop circuit 15, and the D-flip-flop circuit 16. The input data "da-1-24" of 24-bits [[are]] is inputted into the first data polarity inversion determination circuit 11 and also inputted into D-terminals of the D-flip-flop circuits 13-1, 13-2, ---, 13-24. The D-flip-flop circuits 13-1, 13-2, ---, 13-24 latch[[es]] the input data "da-1-24" of 24-bits in ~~synchronizing~~ synchronization with the failing edges of the clock signal "clk", and output data "db-1-24" of 24-bits [[are]] is outputted from Q-terminals of the D-flip-flop circuits 13-1, 13-2, ---, 13-24.

Please replace the paragraph at page 104, lines 2-6, with the following amended paragraph:

The data polarity inversion signal "inv1" is inputted into a D-terminal of the D-flip-flop circuit 15. The D-flip-flop circuit 15 latches the data polarity inversion signal "inv1" in ~~synchronizing~~ synchronization with the failing edges of the clock signal "clk" and outputs a data polarity inversion signal "inv2".

Please replace the paragraph at page 104, lines 7-11, with the following amended paragraph:

The data polarity inversion signal "inv2" is inputted into a D-terminal of the D-flip-flop circuit 16. The D-flip-flop circuit 16 latches the data polarity inversion signal "inv2" in ~~synchronizing~~ synchronization with the falling edges of the clock signal "clk" and outputs a data polarity inversion signal "inv3".

Please replace the paragraph at page 105, lines 12-17, with the following amended paragraph:

The inverted data "dc-1-24" of 24-bits [[are]] is inputted into D-terminals of the D-flip-flop circuits 14-1, 14-2, ---, 14-24. The D-flip-flop circuits 14-1, 14-2, ---, 14-24 latch[[es]] the input data "dc-1-24" of 24-bits in ~~synchronizing~~ synchronization with the falling edges of the clock signal "clk", and output data "dd-1-24" of 24-bits [[are]] is outputted from Q-terminals of the D-flip-flop circuits [[134]]14-1, 14-2, ---, 14-24.

Please replace the paragraph at page 105, line 18 - page 106, line 3, with the following amended paragraph:

FIG. 35 is a timing chart illustrative of waveforms of the clock signal "clk", the data "da-1-24", the data "db-1-24", the data "dc-1-24", [[and]] the data "dd-1-24", and the data polarity inversion signals "inv2" and "inv3" shown in FIG. 34. Prior to a time "t1", all 24-bits of the

input data "da-1-24" are high level "H" or "1". At the time "t1", all 24-bits of the input data "da-1-24" are changed from the high level to the low level "L" or "0" in ~~synchronizing~~ synchronization with the rising edge of the clock signal "clk". At a time "t3", all 24-bits of the input data "da-1-24" are changed from the low level to the high level "H" or "1" in ~~synchronizing~~ synchronization with the rising edge of the clock signal "clk".

Please replace the paragraph at page 106, lines 4-12, with the following amended paragraph:

The input data "da-1-24" [[are]] is inputted into the D-flip-flop circuits 13-1, 13-2, 13-3, --, 13-24. The D-flip-flop circuits 13-1, 13-2, 13-3, ---, 13-24 output the output data "db-1-24". Prior to a time "t2", all 24-bits of the output data "db-1-24" are high level "H" or "1". At the time "t2", all 24-bits of the output data "db-1-24" are changed from the high level to the low level "L" or "0" in ~~synchronizing~~ synchronization with the falling edge of the clock signal "clk". At a time "t4", all 24-bits of the output data "db-1-24" are changed from the low level to the high level "H" or "1" in ~~synchronizing~~ synchronization with the falling edge of the clock signal "clk".

Please replace the paragraph at page 107, lines 14-18, with the following amended paragraph:

The data "dc-1-24" are latched by the D-flip-flop circuits 14-1, 14-2, ---, 14-24 in ~~synchronizing~~ synchronization with the falling edges of the clock signal "clk", and data "dd-1-

24" outputted from the D-flip-flop circuits 14-1, 14-2, ---, 14-24. All 24-bits of the data "dd-1-

24" outputted from the D-flip-flop circuits 14-1, 14-2, ---, 14-24 remain high level "H" or "1".

Please delete the present Abstract of the Disclosure.

Please add the following new Abstract of the Disclosure:

A method of driving a liquid crystal display device includes: branching original image data having an original data rate into branched plural-systems image data comprising plural systems having a converted data rate that is equal to either said original data rate or a half of said original data rate; supplying a source driver circuit with said branched plural-systems image data in synchronization with at least one clock signal having a clock frequency that is a quarter of said original data rate; and allowing said source driver circuit to further branch said branched plural-systems image data into gray-scale voltage signals. Circuitry for driving the liquid crystal display device may include: a timing controller; a plurality of data bus lines; and a plurality of source driver circuits for incorporating said image data in synchronization with said at least one clock signal and converting said image data into gray-scale voltage signals.